Lab 5: Datapath/Control Unit Integration and system testing

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Objective

The objective of this lab is to design the entire control unit using entities from previous labs. The main components used will be the next-address unit, opcode unit, PC-register, Instruction cache, register file, ALU, sign extension and data cache. Using all these components, the data path interconnecting all these components together will be designed.

Procedure

The CPU designed will have all the main instructions that the MIPS CPU offers. A signal coming from the output of the icache unit will be routed to the opcode unit which defines all the inputs for all the units designed in previous labs.

Results

For the designed methodology, it was decided that a port map would be used to bring the entire circuit together. There are 7 components that will be used together plus an 8th circuit.vhd component. The components are as follows:

- Next_address: this component contains the next address unit.
- Opcoderoute: this component takes in the opcode and outputs all the inputs necessary for all other units.
- Pc_icache: this component contains the program counter, the ICACHE register AS WELL as the mux that decides between rt and rd for the destination register.
- Regfile: This component contains the register file.
- Signextension_mux: this component contains the sign extension component as well as the mux routes to the y of the ALU input.
- ALU: this component is the ALU that performs all the arithmetic functions
- Datacache: this is the component that saves results outputted by the ALU and ALSO the mux that takes in the outputs of the ALU and datacache.

Finally, using a portmap (circuit.vhd), all these components are interconnected. Below, all the code will be shown.

Next_address

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;
entity next_address is
port(rt, rs : in std_logic_vector(31 downto 0);
 -- two register inputs
        pc : in std_logic_vector(31 downto 0);
        target_address : in std_logic_vector(25 downto 0);
        branch_type : in std_logic_vector(1 downto 0);
        pc_sel : in std_logic_vector(1 downto 0);
        next_pc : out std_logic_vector(31 downto 0));
end next_address ;
```

```
architecture next_add_arch of next_address is
	signal branch_offset: std_logic_vector(31 downto 0);
begin

inpuediting:process(pc, target_address)
begin

	if (target_address(15) = '0') then --sign extension branch_offset
		branch_offset(31 downto 16) <= (others => '0');
		branch_offset(15 downto 0) <= target_address(15 downto 0);
	else --sign extension branch_offset
		branch_offset(31 downto 16) <= (others => '1');
		branch_offset(15 downto 0) <= target_address(15 downto 0);
	end if;
end process inpuediting;

--pc_inc <= pc + "00000000000000000000000000000001";

PCMUX:process(pc_sel, branch_type, rs, rt, branch_offset, target_address, pc)
begin
	case pc_sel is
		when "00" =>
			case branch_type is
				when "01" => --beq
					if (rs = rt) then
						next_pc <= pc +
"00000000000000000000000000000001" + branch_offset(31 downto 0);
					end if;
				when "10" => --bne
					if (rs /= rt) then
						next_pc<= pc +
"00000000000000000000000000000001" + branch_offset(31 downto 0);
					end if;
				when "11" => --bltz
					if (rs(31) = '1') then
						next_pc <= pc +
"00000000000000000000000000000001" + branch_offset(31 downto 0);
					end if;
				when "00" => --pc increment
					next_pc <= pc + "00000000000000000000000000000001";
				when others =>
			end case;
		when "01" => --jump address
```

```
                    next_pc <= "000000" & target_address;
                when "10" => --jump rs
                    next_pc <= rs;
                when others => --next_pc = pc
                    next_pc <= pc;
        end case;
end process PCMUX;

end next_add_arch;
```

Opcoderoute

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_signed.all;

entity opcoderoute is
port(
        icacheout_combin : in std_logic_vector(31 downto 0);
        reg_write, reg_dst, reg_in_src, alu_src, add_sub, data_write: out std_logic;
        logic_func, alu_func, sign_extend_func, branch_type, pc_sel: out std_logic_vector(1 downto 0));
end opcoderoute;

architecture opcoderoute_arch of opcoderoute is
begin

process(icacheout_combin)
begin
case icacheout_combin(31 downto 26) is
                when "001111" => --lui
                    reg_write <= '1';
                    reg_dst <= '0';
                    reg_in_src <= '1';
                    alu_src <= '1';
                    add_sub <= '0';
                    data_write <= '0';
                    logic_func <= "00";
                    alu_func <= "00";
                    sign_extend_func <= "00";
                    branch_type <= "00";
                    pc_sel <= "00";
                when "000000" =>
                    case icacheout_combin(5 downto 0) is
                            when "100000" => --add
```

```
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '0';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "10";
            sign_extend_func <= "10";
            branch_type <= "00";
            pc_sel <= "00";
        when "100010" => --sub
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "10";
            sign_extend_func <= "10";
            branch_type <= "00";
            pc_sel <= "00";
        when "101010" => --slt
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "01";
            sign_extend_func <= "01";
            branch_type <= "10";
            pc_sel <= "00";
        when "100100" => --and
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "11";
```

```
            sign_extend_func <= "11";
            branch_type <= "00";
            pc_sel <= "00";
        when "100101" => --or
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "01";
            alu_func <= "11";
            sign_extend_func <= "11";
            branch_type <= "00";
            pc_sel <= "00";
        when "100110" => --xor
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "10";
            alu_func <= "11";
            sign_extend_func <= "11";
            branch_type <= "00";
            pc_sel <= "00";
        when "100111" => --nor
            reg_write <= '1';
            reg_dst <= '1';
            reg_in_src <= '1';
            alu_src <= '0';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "11";
            alu_func <= "11";
            sign_extend_func <= "11";
            branch_type <= "00";
            pc_sel <= "00";
        when "001000" => --jr
            reg_write <= '0';
            reg_dst <= '0';
            reg_in_src <= '0';
            alu_src <= '0';
```

```
                add_sub <= '0';
                data_write <= '0';
                logic_func <= "00";
                alu_func <= "00";
                sign_extend_func <= "00";
                branch_type <= "11";
                pc_sel <= "00";
            when others =>
        end case;
when "001000" => --addi
        reg_write <= '1';
        reg_dst <= '0';
        reg_in_src <= '1';
        alu_src <= '1';
        add_sub <= '0';
        data_write <= '0';
        logic_func <= "00";
        alu_func <= "10";
        sign_extend_func <= "10";
        branch_type <= "00";
        pc_sel <= "00";
when "001010" => --slti
        reg_write <= '1';
        reg_dst <= '0';
        reg_in_src <= '1';
        alu_src <= '1';
        add_sub <= '0';
        data_write <= '0';
        logic_func <= "00";
        alu_func <= "10";
        sign_extend_func <= "10";
        branch_type <= "00";
        pc_sel <= "00";
when "001100" => --andi
        reg_write <= '1';
        reg_dst <= '0';
        reg_in_src <= '1';
        alu_src <= '1';
        add_sub <= '1';
        data_write <= '0';
        logic_func <= "00";
        alu_func <= "11";
        sign_extend_func <= "11";
        branch_type <= "00";
```

```
            pc_sel <= "00";
        when "001101" => --ori
            reg_write <= '1';
            reg_dst <= '0';
            reg_in_src <= '1';
            alu_src <= '1';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "01";
            alu_func <= "11";
            sign_extend_func <= "11";
            branch_type <= "00";
            pc_sel <= "00";
        when "001110" => --xori
            reg_write <= '1';
            reg_dst <= '0';
            reg_in_src <= '1';
            alu_src <= '1';
            add_sub <= '1';
            data_write <= '0';
            logic_func <= "10";
            alu_func <= "11";
            sign_extend_func <= "11";
            branch_type <= "00";
            pc_sel <= "00";
        when "100011" => --lw
            reg_write <= '1';
            reg_dst <= '0';
            reg_in_src <= '0';
            alu_src <= '1';
            add_sub <= '0';
            data_write <= '0';
            logic_func <= "10";
            alu_func <= "10";
            sign_extend_func <= "10";
            branch_type <= "00";
            pc_sel <= "00";
        when "101011" => --sw
            reg_write <= '0';
            reg_dst <= '0';
            reg_in_src <= '0';
            alu_src <= '1';
            add_sub <= '0';
            data_write <= '1';
```

```
            logic_func <= "10";
            alu_func <= "10";
            sign_extend_func <= "10";
            branch_type <= "00";
            pc_sel <= "00";
        when "000010" => --j
            reg_write <= '0';
            reg_dst <= '0';
            reg_in_src <= '0';
            alu_src <= '0';
            add_sub <= '0';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "00";
            sign_extend_func <= "00";
            branch_type <= "00";
            pc_sel <= "01";
        when "000001" => --bltz
            reg_write <= '0';
            reg_dst <= '0';
            reg_in_src <= '0';
            alu_src <= '0';
            add_sub <= '0';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "00";
            sign_extend_func <= "00";
            branch_type <= "11";
            pc_sel <= "00";
        when "000100" => --beq
            reg_write <= '0';
            reg_dst <= '0';
            reg_in_src <= '0';
            alu_src <= '0';
            add_sub <= '0';
            data_write <= '0';
            logic_func <= "00";
            alu_func <= "00";
            sign_extend_func <= "00";
            branch_type <= "11";
            pc_sel <= "00";
        when "000101" => --bne
            reg_write <= '0';
            reg_dst <= '0';
```

```
                        reg_in_src <= '0';
                        alu_src <= '0';
                        add_sub <= '0';
                        data_write <= '0';
                        logic_func <= "00";
                        alu_func <= "00";
                        sign_extend_func <= "00";
                        branch_type <= "10";
                        pc_sel <= "00";
                when others =>
end case;
end process;
end opcoderoute_arch;
```

PC_icache

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
--use IEEE.std_logic_signed.all;

entity pc_icache is
port(
        clk, reset, reg_dst : in std_logic;
        nextaddressout_pcin : in std_logic_vector(31 downto 0);
        instruction : out std_logic_vector (31 downto 0);
        pcout : out std_logic_vector(31 downto 0);
        instruction_target_address : out std_logic_vector(25 downto 0);
        output_address_regfile : out std_logic_vector(4 downto 0);
        rs_out, rt_out, rd_out : out std_logic_vector(4 downto 0);
        immediate_out : out std_logic_vector(15 downto 0));
end pc_icache ;

architecture pc_i_cache of pc_icache is
        signal pc : std_logic_vector(31 downto 0);
        --signal icache_address : std_logic_vector(4 downto 0);
        signal machine_code_instruction : std_logic_vector(31 downto 0);
begin

pcout <= pc;
instruction <= machine_code_instruction;
instruction_target_address <= machine_code_instruction(25 downto 0);

pcregister: process(clk,reset,nextaddressout_pcin)
begin
```

```
                        if (reset = '1') then
                                pc <= (others => '0');
                        elsif (clk'event and clk ='1') then
                                pc <= nextaddressout_pcin;
                        end if;
end process pcregister;


icache: process(pc)
begin
        case pc(4 downto 0) is
                when "00000" =>
                        machine_code_instruction <= "00111100000000010111011101110111"; -- lui
r1, 0111011101110111
                when "00001" =>
                        machine_code_instruction <= "00000000001000000001000000100000"; -- add
r2, r1, r0
                when "00010" =>
                        machine_code_instruction <= "00111100000000110000111100001111"; -- lui
r3, 0000111100001111
                when "00011" =>
                        machine_code_instruction <= "00000000001000110010000000100010"; -- sub
r4, r1, r3
                when "00100" =>
                        machine_code_instruction <= "00000000000000110010100000101010"; -- slt
r5, r0, r3
                when "00101" =>
                        machine_code_instruction <= "00100000011001100000000011111111"; -- addi
r6, r3 , 0000000011111111
                when "00110" =>
                        machine_code_instruction <= "00101000011001100000000000000000"; -- slti
r6, r3, 0000000000000000
                when "00111" =>
                        machine_code_instruction <= "00000000001000110011000000100100"; -- and
r6, r1, r3
                when "01000" =>
                        machine_code_instruction <= "00000000001000110011000000100101"; -- or
r6, r1, r3
                when "01001" =>
                        machine_code_instruction <= "00000000001000110011000000100110"; -- xor
r6, r1, r3
                when "01010" =>
                        machine_code_instruction <= "00000000001000110011000000100111"; -- nor
r6, r1, r3
```

```
                when "01011" =>
                        machine_code_instruction <= "00110000011001101111000011110000"; -- andi
r6, r3, 1111000011110000
                when "01100" =>
                        machine_code_instruction <= "00110100011001101111000011110000"; -- ori
r6, r3, 1111000011110000
                when "01101" =>
                        machine_code_instruction <= "00111000011001100101010101010101"; -- xori
r6, r3, 0101010101010101
                when "01110" =>
                        machine_code_instruction <= "10001100101001100101010101010101"; -- lw
r6, 0101010101010101(r5)
                when "01111" =>
                        machine_code_instruction <= "10101100100001100101010101010101"; -- sw
r6, 0101010101010101(r4)
                when "10000" =>
                        machine_code_instruction <= "00001000000000000000000000010010"; -- j
10010
                when "10001" =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
                when "10010" =>
                        machine_code_instruction <= "00100000000010010000000000010101"; -- addi
r9, r0, 0000000000010101
                when "10011" =>
                        machine_code_instruction <= "00001000000000000000000000010101"; -- jr r9
                when "10100" =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
                when "10101" =>
                        machine_code_instruction <= "00000100010000000000000000010111"; --
        bltz r2, 10111
                when "10110" =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
                when "10111" =>
                        machine_code_instruction <= "00010000000010100000000000011001"; -- beq
r0, r10, 11001
                when "11000" =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
                when "11001" =>
                        machine_code_instruction <= "00010100001000100000000000011011"; -- bne
r1, r2, 11011
```

```
                when "11010" =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
                when "11011" =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
                when others =>
                        machine_code_instruction <= "00000000000000000000000000000000"; -- do
nothing
        end case;
end process icache;

rs_rt_etc_out: process(machine_code_instruction)
begin
        rs_out<=machine_code_instruction(25 downto 21);
        rt_out<=machine_code_instruction(20 downto 16);
        rd_out<=machine_code_instruction(15 downto 11);
        immediate_out<=machine_code_instruction(15 downto 0);
end process rs_rt_etc_out;

mux: process(reg_dst,machine_code_instruction)
begin
        case reg_dst is
                when '0' => --rt
                        output_address_regfile <= machine_code_instruction(20 downto 16);
                when '1' => --rd
                        output_address_regfile <= machine_code_instruction(15 downto 11);
                when others =>
        end case;
end process mux;

end pc_i_cache;
```

Regfile

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity regfile is
port( din : in std_logic_vector(31 downto 0);
                reset : in std_logic;
                clk : in std_logic;
                write : in std_logic;
                read_a : in std_logic_vector(4 downto 0);
```

```
                read_b : in std_logic_vector(4 downto 0);
                write_address : in std_logic_vector(4 downto 0);
                out_a : out std_logic_vector(31 downto 0);
                out_b : out std_logic_vector(31 downto 0));
end regfile ;

architecture unti of regfile is

        type registerfile is array (31 downto 0) of std_logic_vector(31 downto 0);-- := (others => (others
=> '0'));

        signal bitreg : registerfile := (others => (others => '0'));

begin

        out_a <=  bitreg(conv_integer(read_a));
        out_b <=  bitreg(conv_integer(read_b));

        writing:process(reset, clk, write)
        begin
                if (reset = '1') then
                        bitreg(0) <= (others => '0');
                        bitreg(1) <= (others => '0');
                        bitreg(2) <= (others => '0');
                        bitreg(3) <= (others => '0');
                        bitreg(4) <= (others => '0');
                        bitreg(5) <= (others => '0');
                        bitreg(6) <= (others => '0');
                        bitreg(7) <= (others => '0');
                        bitreg(8) <= (others => '0');
                        bitreg(9) <= (others => '0');
                        bitreg(10) <= (others => '0');
                        bitreg(11) <= (others => '0');
                        bitreg(12) <= (others => '0');
                        bitreg(13) <= (others => '0');
                        bitreg(14) <= (others => '0');
                        bitreg(15) <= (others => '0');
                        bitreg(16) <= (others => '0');
                        bitreg(17) <= (others => '0');
                        bitreg(18) <= (others => '0');
                        bitreg(19) <= (others => '0');
                        bitreg(20) <= (others => '0');
                        bitreg(21) <= (others => '0');
                        bitreg(22) <= (others => '0');
```

```
                bitreg(23) <= (others => '0');
                bitreg(24) <= (others => '0');
                bitreg(25) <= (others => '0');
                bitreg(26) <= (others => '0');
                bitreg(27) <= (others => '0');
                bitreg(28) <= (others => '0');
                bitreg(29) <= (others => '0');
                bitreg(30) <= (others => '0');
                bitreg(31) <= (others => '0');
        elsif(write ='1' and clk'event and clk='1') then
                bitreg(conv_integer(write_address)) <= din;
        end if;
    end process;

end unti;
```

Signextension_mux

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_signed.all;

entity signextension_mux is
port(
    func : in std_logic_vector(1 downto 0);
    immediate : in std_logic_vector(15 downto 0);
    out_b_input : in std_logic_vector(31 downto 0);
    alu_src : in std_logic;
    muxout_aluin : out std_logic_vector(31 downto 0));
end signextension_mux;

architecture sign_extension of signextension_mux is
    signal sign_extension_output : std_logic_vector(31 downto 0);
begin

signextensionblock: process(immediate, func)
begin
    case func is
        when "00" =>
            sign_extension_output(15 downto 0) <= (others => '0');
            sign_extension_output(31 downto 16) <= immediate;
        when "01" =>
            sign_extension_output(15 downto 0) <= immediate;
            sign_extension_output(31 downto 16) <= (others => immediate(15));
```

```
                when "10" =>
                        sign_extension_output(15 downto 0) <= immediate;
                        sign_extension_output(31 downto 16) <= (others => immediate(15));
                when "11" =>
                        sign_extension_output(15 downto 0) <= immediate;
                        sign_extension_output(31 downto 16) <= (others => '0');
                when others =>
        end case;
end process signextensionblock;

mux: process(sign_extension_output, out_b_input, alu_src)
begin
        if (alu_src = '0') then
                muxout_aluin <= out_b_input;
        else
                muxout_aluin <= sign_extension_output;
        end if;
end process mux;

end sign_extension;
```

ALU

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_signed.all;


entity ALU is
port(x, y : in std_logic_vector(31 downto 0);
        add_sub : in std_logic;
        logic_func : in std_logic_vector(1 downto 0);
        func : in std_logic_vector(1 downto 0);
        output : out std_logic_vector(31 downto 0);
        overflow : out std_logic;
        zero : out std_logic);
end ALU;

architecture calc of ALU is
        signal logic_unit_output, add_subtract_output: std_logic_vector(31 downto 0);

begin
        outputmux: process(func, add_subtract_output, logic_unit_output, y)
                begin
```

```
                        case func is
                                when "00" =>
                                        output <= y;
                                when "01" =>
                                        output <= "00000000000000000000000000000000" &
add_subtract_output(31);
                                when "10" =>
                                        output <= add_subtract_output;
                                when "11" =>
                                        output <= logic_unit_output;
                                when others =>
                                        null;
                        end case;
        end process outputmux;

        logicunit: process(logic_func, x, y)
                begin
                        case logic_func is
                                when "00" =>
                                        logic_unit_output <= x and y;
                                when "01" =>
                                        logic_unit_output <= x or y;
                                when "10" =>
                                        logic_unit_output <= x xor y;
                                when "11" =>
                                        logic_unit_output <= x nor y;
                                when others =>
                                        logic_unit_output <= (others => '0');
                        end case;
        end process logicunit;

        adder_subtract: process(y, x, add_sub)
                begin
                        if add_sub = '0' then
                                add_subtract_output <= x + y;
                        elsif add_sub = '1' then
                                add_subtract_output <= x - y;
                        else
                                null;
                        end if;
        end process adder_subtract;

        zeroreg: process(add_subtract_output)
                begin
```

```
                if (unsigned(add_subtract_output) = 0) then
                        zero <= '1';
                else
                        zero <= '0';
                end if;
        end process zeroreg;

        overflowreg: process(x, y, add_subtract_output, add_sub)
                begin
                        case add_sub is
                                when '0' =>
                                        if (x(31) = '0' and y(31) = '0' and add_subtract_output(31) = '1')
then
                                                overflow <= '1';
                                        elsif (x(31) = '1' and y(31) = '1' and add_subtract_output(31) =
'0') then
                                                overflow <= '1';
                                        else
                                                overflow <= '0';
                                        end if;
                                when '1' =>
                                        if (x(31) = '1' and y(31) = '0' and add_subtract_output(31) = '0')
then
                                                overflow <= '1';
                                        elsif (x(31) = '0' and y(31) = '1' and add_subtract_output(31) =
'1') then
                                                overflow <= '1';
                                        else
                                                overflow <='0';
                                        end if;
                                when others =>
                                        null;
                        end case;
        end process overflowreg;

end;
```

Datacache

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_signed.all;

entity datacache is
```

```
port(
	clk, reset, data_write, reg_in_src : in std_logic;
	mux_d_output : out std_logic_vector(31 downto 0);
	d_cache_in : in std_logic_vector(31 downto 0);
	aluout_dcachein : in std_logic_vector(31 downto 0));
end datacache;

architecture data_c_arch of datacache is
	type dcache is array (31 downto 0) of std_logic_vector(31 downto 0);

	signal d_cache : dcache := (others => (others => '0'));
	signal d_cache_address : std_logic_vector(4 downto 0);
	signal d_cache_out : std_logic_vector(31 downto 0);
begin

d_cache_address <= aluout_dcachein(4 downto 0);

data_cache:process(clk, reset,d_cache_in)
begin
		if (reset = '1') then
			d_cache(0) <= (others => '0');
			d_cache(1) <= (others => '0');
			d_cache(2) <= (others => '0');
			d_cache(3) <= (others => '0');
			d_cache(4) <= (others => '0');
			d_cache(5) <= (others => '0');
			d_cache(6) <= (others => '0');
			d_cache(7) <= (others => '0');
			d_cache(8) <= (others => '0');
			d_cache(9) <= (others => '0');
			d_cache(10) <= (others => '0');
			d_cache(11) <= (others => '0');
			d_cache(12) <= (others => '0');
			d_cache(13) <= (others => '0');
			d_cache(14) <= (others => '0');
			d_cache(15) <= (others => '0');
			d_cache(16) <= (others => '0');
			d_cache(17) <= (others => '0');
			d_cache(18) <= (others => '0');
			d_cache(19) <= (others => '0');
			d_cache(20) <= (others => '0');
			d_cache(21) <= (others => '0');
			d_cache(22) <= (others => '0');
			d_cache(23) <= (others => '0');
```

```
                        d_cache(24) <= (others => '0');
                        d_cache(25) <= (others => '0');
                        d_cache(26) <= (others => '0');
                        d_cache(27) <= (others => '0');
                        d_cache(28) <= (others => '0');
                        d_cache(29) <= (others => '0');
                        d_cache(30) <= (others => '0');
                        d_cache(31) <= (others => '0');
                elsif (clk'event and clk ='1' and data_write = '1') then
                        d_cache(conv_integer(d_cache_address)) <= d_cache_in;
                end if;
end process data_cache;

d_cache_mux:process(reg_in_src,d_cache_address,aluout_dcachein)
begin
        if (reg_in_src = '0') then
                mux_d_output <= d_cache(conv_integer(d_cache_address));
        else
                mux_d_output <= aluout_dcachein;
        end if;
end process d_cache_mux;

end data_c_arch;
```

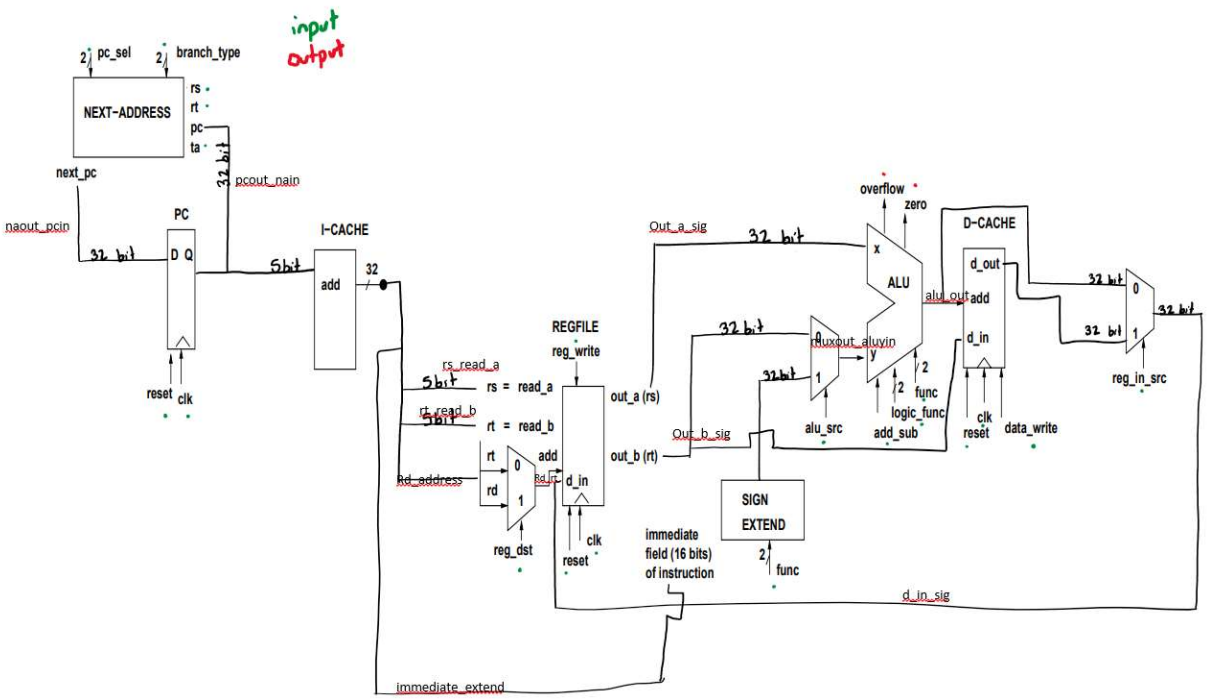
Circuit.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_signed.all;
entity cpu is
port(reset : in std_logic;
 clk : in std_logic;
 rs_out, rt_out : out std_logic_vector(3 downto 0); -- output ports from register file
 pc_out : out std_logic_vector(3 downto 0); -- pc reg
 overflow, zero : out std_logic);
end cpu;

architecture cpu5 of cpu is
--components
component next_address
port(rt, rs : in std_logic_vector(31 downto 0);
        pc : in std_logic_vector(31 downto 0);
        target_address : in std_logic_vector(25 downto 0);
        branch_type : in std_logic_vector(1 downto 0);
```

```
        pc_sel : in std_logic_vector(1 downto 0);
        next_pc : out std_logic_vector(31 downto 0));
end component;

component pc_icache --ADD AN OUTPUT FOR OPCODEROUTE
port(

        clk, reset, reg_dst : in std_logic;
        nextaddressout_pcin : in std_logic_vector(31 downto 0);
        instruction : out std_logic_vector (31 downto 0);
        pcout : out std_logic_vector(31 downto 0);
        instruction_target_address : out std_logic_vector(25 downto 0);
        output_address_regfile : out std_logic_vector(4 downto 0);
        rs_out, rt_out, rd_out : out std_logic_vector(4 downto 0);
        immediate_out : out std_logic_vector(15 downto 0));
end component;

component regfile
port( din : in std_logic_vector(31 downto 0);
                reset : in std_logic;
                clk : in std_logic;
                write : in std_logic;
                read_a : in std_logic_vector(4 downto 0);
                read_b : in std_logic_vector(4 downto 0);
                write_address : in std_logic_vector(4 downto 0);
                out_a : out std_logic_vector(31 downto 0);
                out_b : out std_logic_vector(31 downto 0));
end component;

component signextension_mux
port(
        func : in std_logic_vector(1 downto 0);
        immediate : in std_logic_vector(15 downto 0);
        out_b_input : in std_logic_vector(31 downto 0);
        alu_src : in std_logic;
        muxout_aluin : out std_logic_vector(31 downto 0));
end component;

component ALU
port(x, y : in std_logic_vector(31 downto 0);
        add_sub : in std_logic;
        logic_func : in std_logic_vector(1 downto 0);
        func : in std_logic_vector(1 downto 0);
        output : out std_logic_vector(31 downto 0);
```

```
        overflow : out std_logic;
        zero : out std_logic);
end component;

component datacache
port(
        clk, reset, data_write, reg_in_src : in std_logic;
        mux_d_output : out std_logic_vector(31 downto 0);
        d_cache_in : in std_logic_vector(31 downto 0);
        aluout_dcachein : in std_logic_vector(31 downto 0));
end component;

component opcoderoute
port(
        icacheout_combin : in std_logic_vector(31 downto 0);
        reg_write, reg_dst, reg_in_src, alu_src, add_sub, data_write: out std_logic;
        logic_func, alu_func, sign_extend_func, branch_type, pc_sel: out std_logic_vector(1 downto 0));
end component;

--signal

signal insig_pc_sel, insig_branch_type, insig_func_sign, insig_func_alu, insig_logic_func :
std_logic_vector(1 downto 0);
signal insig_reset, insig_clk, insig_reg_dst, insig_reg_write, insig_alu_src, insig_add_sub,
insig_data_write, insig_reg_in_src : std_logic;
signal insig_ta : std_logic_vector(25 downto 0);

signal iout_opcoderoute, pcout_nain, naout_pcin, d_in_sig, out_a_sig, out_b_sig, muxout_aluyin,
alu_out: std_logic_vector(31 downto 0);

signal rd_rt, rs_read_a, rt_read_b, rd_address: std_logic_vector(4 downto 0);

signal immediate_extend: std_logic_vector(15 downto 0);

--signal iout_opcoderoute, pcout_nain,naout_pcin,d_in_sig,out_a_sig,out_b_sig,muxout_aluyin,alu_out
: std_logic_vector(31 downto 0);
--signal rd_rt, rs_read_a, rt_read_b, rd_address : std_logic_vector(4 downto 0);
--signal immediate_extend: std_logic_vector(15 downto 0);


for U1: next_address use entity WORK.next_address(next_add_arch);
for U2: pc_icache use entity WORK.pc_icache(pc_i_cache);
for U3: regfile use entity WORK.regfile(unti);
for U4: signextension_mux use entity WORK.signextension_mux(sign_extension);
```

```
for U5: ALU use entity WORK.ALU(calc);
for U6: datacache use entity WORK.datacache(data_c_arch);
for U7: opcoderoute use entity WORK.opcoderoute(opcoderoute_arch);

begin

rs_out <= out_a_sig(3 downto 0);
rt_out <= out_b_sig(3 downto 0);
pc_out <= pcout_nain(3 downto 0);


U1: next_address port map (rt => out_b_sig, rs=> out_a_sig, pc=> pcout_nain, target_address=>
insig_ta, branch_type=> insig_branch_type, pc_sel=> insig_pc_sel, next_pc=> naout_pcin);
U2: pc_icache port map (clk => clk, reset => reset, reg_dst => insig_reg_dst, nextaddressout_pcin =>
naout_pcin, instruction => iout_opcoderoute, pcout=>pcout_nain, output_address_regfile => rd_rt,
rs_out => rs_read_a, rt_out => rt_read_b, rd_out => rd_address, immediate_out => immediate_extend,
instruction_target_address => insig_ta);
U3: regfile port map (din => d_in_sig, reset => reset, clk => clk, write => insig_reg_write, read_a =>
rs_read_a, read_b => rt_read_b, write_address => rd_rt, out_a => out_a_sig, out_b => out_b_sig);
U4: signextension_mux port map (func => insig_func_sign, immediate => immediate_extend,
out_b_input => out_b_sig, alu_src => insig_alu_src, muxout_aluin => muxout_aluyin);
U5: ALU port map (x => out_a_sig, y => muxout_aluyin, add_sub => insig_add_sub, logic_func =>
insig_logic_func, func => insig_func_alu, output => alu_out, overflow => overflow, zero => zero);
U6: datacache port map (clk => clk, reset => reset, data_write => insig_data_write, reg_in_src =>
insig_reg_in_src, mux_d_output => d_in_sig, d_cache_in => out_b_sig, aluout_dcachein => alu_out);
U7: opcoderoute port map (icacheout_combin => iout_opcoderoute, reg_write => insig_reg_write,
reg_dst => insig_reg_dst, reg_in_src => insig_reg_in_src, alu_src => insig_alu_src, add_sub =>
insig_add_sub, data_write => insig_data_write, logic_func => insig_logic_func, alu_func =>
insig_func_alu, sign_extend_func => insig_func_sign, branch_type => insig_branch_type, pc_sel =>
insig_pc_sel);
end cpu5;
```


input
output
2 pc_sel
2 branch_type
NEXT-ADDRESS
rs
rt
pc
ta
32 bit
pcout_nain
next_pc
naout_pcin
PC
32 bit
D Q
5bit
I-CACHE
add
32
reset
clk
REGFILE
reg_write
rs_read_a
5bit
rs = read_a
rt_read_b
5bit
rt = read_b
rt
rd
0
1
reg_dst
Rd_address
add
d_in
reset
clk
out_a (rs)
out_b (rt)
Out_a_sig
Out_b_sig
32 bit
overflow
zero
x
ALU
y
alu_out
32 bit
0
1
alu_src
2
func
logic_func
add_sub
D-CACHE
d_out
add
d_in
clk
reset
data_write
32 bit
0
1
32 bit
reg_in_src
SIGN
EXTEND
immediate
field (16 bits)
of instruction
2
func
d_in_sig
immediate_extend

Modelsim Simulation

Opcoderoute

Attached at end of document: opcode.pdf

CPU

Attached at end of document: CPU0-23.pdf, CPU23-46.pdf

Directory Listing

[grace] [/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1] > pwd

/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1

[grace] [/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1] > ls -al cpu.bit

-rw-rw---- 1 o_dabaye o_dabaye 3825888 Dec 8 11:58 cpu.bit

[grace] [/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1] >

Log files

Implementation Design

```
*** Running vivado
    with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb
-mode batch -source cpu.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: link_design -top cpu -part xc7a100tcsg324-1
Design is defaulting to srcset: sources_1
Design is defaulting to constrset: constrs_1
INFO: [Netlist 29-17] Analyzing 306 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
Parsing XDC File
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/constrs_1/import
s/lab5tedstuff/cpu.xdc]
Finished Parsing XDC File
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/constrs_1/import
s/lab5tedstuff/cpu.xdc]
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
```

```
No Unisim elements were transformed.

7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
link_design completed successfully
link_design: Time (s): cpu = 00:00:12 ; elapsed = 00:01:29 . Memory (MB):
peak = 1704.559 ; gain = 330.414 ; free physical = 44229 ; free virtual =
150487
Command: opt_design
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command opt_design

Starting DRC Task
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Project 1-461] DRC finished with 0 Errors
INFO: [Project 1-462] Please refer to the DRC report (report_drc) for more
information.

Time (s): cpu = 00:00:02 ; elapsed = 00:00:04 . Memory (MB): peak = 1777.586
; gain = 73.027 ; free physical = 44222 ; free virtual = 150480

Starting Cache Timing Information Task
INFO: [Timing 38-35] Done setting XDC timing constraints.
Ending Cache Timing Information Task | Checksum: 126f05278

Time (s): cpu = 00:00:16 ; elapsed = 00:01:22 . Memory (MB): peak = 2251.086
; gain = 473.500 ; free physical = 43826 ; free virtual = 150084

Starting Logic Optimization Task

Phase 1 Retarget
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Opt 31-49] Retargeted 0 cell(s).
Phase 1 Retarget | Checksum: 126f05278

Time (s): cpu = 00:00:00.19 ; elapsed = 00:00:00.13 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Phase 2 Constant propagation | Checksum: 126f05278

Time (s): cpu = 00:00:00.22 ; elapsed = 00:00:00.16 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0
cells
```

```
Phase 3 Sweep
Phase 3 Sweep | Checksum: 141806dcc

Time (s): cpu = 00:00:00.26 ; elapsed = 00:00:00.20 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization
Phase 4 BUFG optimization | Checksum: 141806dcc

Time (s): cpu = 00:00:00.30 ; elapsed = 00:00:00.24 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are
BUFGs and removed 0 cells.

Phase 5 Shift Register Optimization
Phase 5 Shift Register Optimization | Checksum: 17b81c0e1

Time (s): cpu = 00:00:00.34 ; elapsed = 00:00:00.27 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and
removed 0 cells

Phase 6 Post Processing Netlist
Phase 6 Post Processing Netlist | Checksum: 17b81c0e1

Time (s): cpu = 00:00:00.34 ; elapsed = 00:00:00.28 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Opt 31-389] Phase Post Processing Netlist created 0 cells and removed
0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.01 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
Ending Logic Optimization Task | Checksum: 17b81c0e1

Time (s): cpu = 00:00:00.35 ; elapsed = 00:00:00.30 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101

Starting Power Optimization Task
INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00
ns.
Ending Power Optimization Task | Checksum: 17b81c0e1

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.06 . Memory (MB): peak =
2251.086 ; gain = 0.000 ; free physical = 43843 ; free virtual = 150101

Starting Final Cleanup Task
Ending Final Cleanup Task | Checksum: 17b81c0e1
```

```
Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 2251.086
; gain = 0.000 ; free physical = 43843 ; free virtual = 150101
INFO: [Common 17-83] Releasing license: Implementation
23 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
opt_design completed successfully
opt_design: Time (s): cpu = 00:00:18 ; elapsed = 00:01:27 . Memory (MB): peak
= 2251.086 ; gain = 546.527 ; free physical = 43843 ; free virtual = 150101
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.05 ; elapsed = 00:00:00.02 .
Memory (MB): peak = 2283.098 ; gain = 0.000 ; free physical = 43836 ; free
virtual = 150095
INFO: [Common 17-1381] The checkpoint
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1/cpu_opt.d
cp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file cpu_drc_opted.rpt -pb
cpu_drc_opted.pb -rpx cpu_drc_opted.rpx
Command: report_drc -file cpu_drc_opted.rpt -pb cpu_drc_opted.pb -rpx
cpu_drc_opted.rpx
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file
/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1/cpu_drc_op
ted.rpt.
report_drc completed successfully
report_drc: Time (s): cpu = 00:00:04 ; elapsed = 00:00:07 . Memory (MB): peak
= 2363.141 ; gain = 80.031 ; free physical = 43798 ; free virtual = 150056
Command: place_design
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.
Running DRC as a precondition to command place_design
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.

Starting Placer Task
```

```
INFO: [Place 30-611] Multithreading enabled for place_design using a maximum
of 8 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 .
Memory (MB): peak = 2363.141 ; gain = 0.000 ; free physical = 43791 ; free
virtual = 150050
Phase 1.1 Placer Initialization Netlist Sorting | Checksum: b411f8e4

Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.03 . Memory (MB): peak =
2363.141 ; gain = 0.000 ; free physical = 43791 ; free virtual = 150050
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 .
Memory (MB): peak = 2363.141 ; gain = 0.000 ; free physical = 43791 ; free
virtual = 150050

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
INFO: [Timing 38-35] Done setting XDC timing constraints.
WARNING: [Place 30-574] Poor placement for routing between an IO pin and
BUFG. This is normally an ERROR but the CLOCK_DEDICATED_ROUTE constraint is
set to FALSE allowing your design to continue. The use of this override is
highly discouraged as it may lead to very poor timing results. It is
recommended that this error condition be corrected in the design.

        clk_IBUF_inst (IBUF.O) is locked to IOB_X0Y82
        clk_IBUF_BUFG_inst (BUFG.I) is provisionally placed by clockplacer on
BUFGCTRL_X0Y0
Resolution: Poor placement of an IO pin and a BUFG has resulted in the router
using a non-dedicated path between the two.  There are several things that
could trigger this DRC, each of which can cause unpredictable clock insertion
delays that result in poor timing.  This DRC could be caused by any of the
following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the
BUFG has not been placed in the same half of the device or SLR as the CCIO-
pin (c) a single ended clock has been placed on the N-Side of a differential
pair CCIO-pin.
Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum:
ab49e252

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.90 . Memory (MB): peak =
2363.141 ; gain = 0.000 ; free physical = 43791 ; free virtual = 150049

Phase 1.3 Build Placer Netlist Model
Phase 1.3 Build Placer Netlist Model | Checksum: c1ef66f6

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.97 . Memory (MB): peak =
2363.141 ; gain = 0.000 ; free physical = 43790 ; free virtual = 150049

Phase 1.4 Constrain Clocks/Macros
Phase 1.4 Constrain Clocks/Macros | Checksum: c1ef66f6
```

```
Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.98 . Memory (MB): peak =
2363.141 ; gain = 0.000 ; free physical = 43790 ; free virtual = 150049
Phase 1 Placer Initialization | Checksum: c1ef66f6

Time (s): cpu = 00:00:02 ; elapsed = 00:00:00.98 . Memory (MB): peak =
2363.141 ; gain = 0.000 ; free physical = 43790 ; free virtual = 150049

Phase 2 Global Placement

Phase 2.1 Floorplanning
Phase 2.1 Floorplanning | Checksum: c1ef66f6

Time (s): cpu = 00:00:02 ; elapsed = 00:00:01 . Memory (MB): peak = 2363.141
; gain = 0.000 ; free physical = 43788 ; free virtual = 150047
WARNING: [Place 46-29] place_design is not in timing mode. Skip physical
synthesis in placer
Phase 2 Global Placement | Checksum: 185fe8405

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43735 ; free virtual = 149994

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros
Phase 3.1 Commit Multi Column Macros | Checksum: 185fe8405

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43735 ; free virtual = 149994

Phase 3.2 Commit Most Macros & LUTRAMs
Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 19e853c7b

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43735 ; free virtual = 149994

Phase 3.3 Area Swap Optimization
Phase 3.3 Area Swap Optimization | Checksum: 17c4092f2

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43735 ; free virtual = 149994

Phase 3.4 Pipeline Register Optimization
Phase 3.4 Pipeline Register Optimization | Checksum: 17c4092f2

Time (s): cpu = 00:00:09 ; elapsed = 00:00:03 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43735 ; free virtual = 149994

Phase 3.5 Small Shape Detail Placement
Phase 3.5 Small Shape Detail Placement | Checksum: 226805c67
```

```
Time (s): cpu = 00:00:10 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43741 ; free virtual = 150000

Phase 3.6 Re-assign LUT pins
Phase 3.6 Re-assign LUT pins | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43741 ; free virtual = 150000

Phase 3.7 Pipeline Register Optimization
Phase 3.7 Pipeline Register Optimization | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43741 ; free virtual = 150000
Phase 3 Detail Placement | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43741 ; free virtual = 150000

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization
Phase 4.1 Post Commit Optimization | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43741 ; free virtual = 150000

Phase 4.2 Post Placement Cleanup
Phase 4.2 Post Placement Cleanup | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43744 ; free virtual = 150002

Phase 4.3 Placer Reporting
Phase 4.3 Placer Reporting | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43744 ; free virtual = 150002

Phase 4.4 Final Placement Cleanup
Phase 4.4 Final Placement Cleanup | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43744 ; free virtual = 150002
Phase 4 Post Placement Optimization and Clean-Up | Checksum: 226805c67

Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43744 ; free virtual = 150002
Ending Placer Task | Checksum: 15694d1b1
```

```
Time (s): cpu = 00:00:11 ; elapsed = 00:00:04 . Memory (MB): peak = 2418.160
; gain = 55.020 ; free physical = 43759 ; free virtual = 150018
INFO: [Common 17-83] Releasing license: Implementation
41 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.
place_design completed successfully
place_design: Time (s): cpu = 00:00:13 ; elapsed = 00:00:09 . Memory (MB):
peak = 2418.160 ; gain = 55.020 ; free physical = 43761 ; free virtual =
150019
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.42 ; elapsed = 00:00:00.16 .
Memory (MB): peak = 2418.160 ; gain = 0.000 ; free physical = 43751 ; free
virtual = 150013
INFO: [Common 17-1381] The checkpoint
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1/cpu_place
d.dcp' has been generated.
INFO: [runtcl-4] Executing : report_io -file cpu_io_placed.rpt
report_io: Time (s): cpu = 00:00:00.08 ; elapsed = 00:00:00.18 . Memory (MB):
peak = 2418.160 ; gain = 0.000 ; free physical = 43750 ; free virtual =
150010
INFO: [runtcl-4] Executing : report_utilization -file
cpu_utilization_placed.rpt -pb cpu_utilization_placed.pb
report_utilization: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.19 .
Memory (MB): peak = 2418.160 ; gain = 0.000 ; free physical = 43758 ; free
virtual = 150017
INFO: [runtcl-4] Executing : report_control_sets -verbose -file
cpu_control_sets_placed.rpt
report_control_sets: Time (s): cpu = 00:00:00.04 ; elapsed = 00:00:00.12 .
Memory (MB): peak = 2418.160 ; gain = 0.000 ; free physical = 43757 ; free
virtual = 150017
Command: route_design
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command route_design
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC PLCK-12] Clock Placer Checks: Poor placement for routing
between an IO pin and BUFG.
Resolution: Poor placement of an IO pin and a BUFG has resulted in the router
using a non-dedicated path between the two.  There are several things that
could trigger this DRC, each of which can cause unpredictable clock insertion
delays that result in poor timing.  This DRC could be caused by any of the
following: (a) a clock port was placed on a pin that is not a CCIO-pin (b)the
BUFG has not been placed in the same half of the device or SLR as the CCIO-
```

```
pin (c) a single ended clock has been placed on the N-Side of a differential
pair CCIO-pin.
 This is normally an ERROR but the CLOCK_DEDICATED_ROUTE constraint is set to
FALSE allowing your design to continue. The use of this override is highly
discouraged as it may lead to very poor timing results. It is recommended
that this error condition be corrected in the design.

        clk_IBUF_inst (IBUF.O) is locked to IOB_X0Y82
        clk_IBUF_BUFG_inst (BUFG.I) is provisionally placed by clockplacer on
BUFGCTRL_X0Y0
INFO: [Vivado_Tcl 4-198] DRC finished with 0 Errors, 1 Warnings
INFO: [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more
information.


Starting Routing Task
INFO: [Route 35-254] Multithreading enabled for route_design using a maximum
of 8 CPUs
Checksum: PlaceDB: c9de98c6 ConstDB: 0 ShapeSum: 8cb638eb RouteDB: 0

Phase 1 Build RT Design
Phase 1 Build RT Design | Checksum: 123263277

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2460.766
; gain = 42.605 ; free physical = 43619 ; free virtual = 149879
Post Restoration Checksum: NetGraph: d4aa2a8a NumContArr: 4e7c07ed
Constraints: 0 Timing: 0

Phase 2 Router Initialization
INFO: [Route 35-64] No timing constraints were detected. The router will
operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints
Phase 2.1 Fix Topology Constraints | Checksum: 123263277

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2467.754
; gain = 49.594 ; free physical = 43588 ; free virtual = 149847

Phase 2.2 Pre Route Cleanup
Phase 2.2 Pre Route Cleanup | Checksum: 123263277

Time (s): cpu = 00:00:24 ; elapsed = 00:00:20 . Memory (MB): peak = 2467.754
; gain = 49.594 ; free physical = 43588 ; free virtual = 149847
 Number of Nodes with overlaps = 0
Phase 2 Router Initialization | Checksum: 10319201a

Time (s): cpu = 00:00:24 ; elapsed = 00:00:21 . Memory (MB): peak = 2478.020
; gain = 59.859 ; free physical = 43577 ; free virtual = 149836

Phase 3 Initial Routing
```

```
Phase 3 Initial Routing | Checksum: f690aa50

Time (s): cpu = 00:00:26 ; elapsed = 00:00:21 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43579 ; free virtual = 149838

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0
 Number of Nodes with overlaps = 246
 Number of Nodes with overlaps = 3
 Number of Nodes with overlaps = 0
Phase 4.1 Global Iteration 0 | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43577 ; free virtual = 149837
Phase 4 Rip-up And Reroute | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43577 ; free virtual = 149837

Phase 5 Delay and Skew Optimization
Phase 5 Delay and Skew Optimization | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43577 ; free virtual = 149837

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter
Phase 6.1 Hold Fix Iter | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43577 ; free virtual = 149837
Phase 6 Post Hold Fix | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43577 ; free virtual = 149837

Phase 7 Route finalize

Router Utilization Summary
  Global Vertical Routing Utilization    = 0.370327 %
  Global Horizontal Routing Utilization  = 0.437837 %
  Routable Net Status*
  *Does not include unroutable nets such as driverless and loadless.
  Run report_route_status for detailed report.
  Number of Failed Nets               = 0
  Number of Unrouted Nets             = 0
  Number of Partially Routed Nets     = 0
  Number of Node Overlaps             = 0
```

```
Congestion Report
North Dir 1x1 Area, Max Cong = 30.6306%, No Congested Regions.
South Dir 1x1 Area, Max Cong = 41.4414%, No Congested Regions.
East Dir 1x1 Area, Max Cong = 39.7059%, No Congested Regions.
West Dir 1x1 Area, Max Cong = 35.2941%, No Congested Regions.

------------------------------
Reporting congestion hotspots
------------------------------
Direction: North
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: South
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: East
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0
Direction: West
----------------
Congested clusters found at Level 0
Effective congestion level: 0 Aspect Ratio: 1 Sparse Ratio: 0

Phase 7 Route finalize | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43577 ; free virtual = 149837

Phase 8 Verifying routed nets

 Verification completed successfully
Phase 8 Verifying routed nets | Checksum: 1183ea04f

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43576 ; free virtual = 149836

Phase 9 Depositing Routes
Phase 9 Depositing Routes | Checksum: d629ab27

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43576 ; free virtual = 149836
INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:29 ; elapsed = 00:00:22 . Memory (MB): peak = 2484.020
; gain = 65.859 ; free physical = 43611 ; free virtual = 149871
```

```
Routing Is Done.
INFO: [Common 17-83] Releasing license: Implementation
54 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.
route_design completed successfully
route_design: Time (s): cpu = 00:00:31 ; elapsed = 00:00:37 . Memory (MB):
peak = 2484.020 ; gain = 65.859 ; free physical = 43611 ; free virtual =
149871
INFO: [Timing 38-480] Writing timing data to binary archive.
Writing placer database...
Writing XDEF routing.
Writing XDEF routing logical nets.
Writing XDEF routing special nets.
Write XDEF Complete: Time (s): cpu = 00:00:00.46 ; elapsed = 00:00:00.20 .
Memory (MB): peak = 2484.020 ; gain = 0.000 ; free physical = 43602 ; free
virtual = 149865
INFO: [Common 17-1381] The checkpoint
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1/cpu_route
d.dcp' has been generated.
INFO: [runtcl-4] Executing : report_drc -file cpu_drc_routed.rpt -pb
cpu_drc_routed.pb -rpx cpu_drc_routed.rpx
Command: report_drc -file cpu_drc_routed.rpt -pb cpu_drc_routed.pb -rpx
cpu_drc_routed.rpx
INFO: [DRC 23-27] Running DRC with 8 threads
INFO: [Coretcl 2-168] The results of DRC are in file
/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1/cpu_drc_ro
uted.rpt.
report_drc completed successfully
report_drc: Time (s): cpu = 00:00:03 ; elapsed = 00:00:06 . Memory (MB): peak
= 2572.062 ; gain = 88.035 ; free physical = 43589 ; free virtual = 149850
INFO: [runtcl-4] Executing : report_methodology -file
cpu_methodology_drc_routed.rpt -pb cpu_methodology_drc_routed.pb -rpx
cpu_methodology_drc_routed.rpx
Command: report_methodology -file cpu_methodology_drc_routed.rpt -pb
cpu_methodology_drc_routed.pb -rpx cpu_methodology_drc_routed.rpx
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [Timing 38-35] Done setting XDC timing constraints.
INFO: [DRC 23-133] Running Methodology with 8 threads
INFO: [Coretcl 2-1520] The results of Report Methodology are in file
/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/impl_1/cpu_method
ology_drc_routed.rpt.
report_methodology completed successfully
INFO: [runtcl-4] Executing : report_power -file cpu_power_routed.rpt -pb
cpu_power_summary_routed.pb -rpx cpu_power_routed.rpx
Command: report_power -file cpu_power_routed.rpt -pb
cpu_power_summary_routed.pb -rpx cpu_power_routed.rpx
WARNING: [Power 33-232] No user defined clocks were found in the design!
Resolution: Please specify clocks using create_clock/create_generated_clock
for sequential elements. For pure combinatorial circuits, please specify a
virtual clock, otherwise the vectorless estimation might be inaccurate
INFO: [Timing 38-35] Done setting XDC timing constraints.
```

```
Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation
66 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.
report_power failed
INFO: [runtcl-4] Executing : report_route_status -file cpu_route_status.rpt -
pb cpu_route_status.pb
INFO: [runtcl-4] Executing : report_timing_summary -max_paths 10 -file
cpu_timing_summary_routed.rpt -pb cpu_timing_summary_routed.pb -rpx
cpu_timing_summary_routed.rpx -warn_on_violation
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type:
min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a
maximum of 8 CPUs
WARNING: [Timing 38-313] There are no user specified timing constraints.
Timing constraints are needed for proper timing analysis.
INFO: [runtcl-4] Executing : report_incremental_reuse -file
cpu_incremental_reuse_routed.rpt
INFO: [Vivado_Tcl 4-545] No incremental reuse to report, no incremental
placement and routing data was found.
INFO: [runtcl-4] Executing : report_clock_utilization -file
cpu_clock_utilization_routed.rpt
INFO: [runtcl-4] Executing : report_bus_skew -warn_on_violation -file
cpu_bus_skew_routed.rpt -pb cpu_bus_skew_routed.pb -rpx
cpu_bus_skew_routed.rpx
INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type:
min_max, Timing Stage: Requireds.
INFO: [Timing 38-191] Multithreading enabled for timing update using a
maximum of 8 CPUs
INFO: [Common 17-206] Exiting Vivado at Wed Dec  8 11:53:46 2021...

*** Running vivado
    with args -log cpu.vdi -applog -m64 -product Vivado -messageDb vivado.pb
-mode batch -source cpu.tcl -notrace


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: open_checkpoint cpu_routed.dcp

Starting open_checkpoint Task

Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.29 . Memory (MB): peak =
1343.129 ; gain = 0.000 ; free physical = 44535 ; free virtual = 150797
INFO: [Netlist 29-17] Analyzing 306 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
```

```
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Timing 38-478] Restoring timing data from binary archive.
INFO: [Timing 38-479] Binary timing data restore complete.
INFO: [Project 1-856] Restoring constraints from binary archive.
INFO: [Project 1-853] Binary constraint restore complete.
Reading XDEF placement.
Reading placer database...
Reading XDEF routing.
Read XDEF File: Time (s): cpu = 00:00:00.26 ; elapsed = 00:00:00.61 . Memory
(MB): peak = 2141.250 ; gain = 0.004 ; free physical = 43808 ; free virtual =
150070
Restored from archive | CPU: 0.620000 secs | Memory: 3.695457 MB |
Finished XDEF File Restore: Time (s): cpu = 00:00:00.26 ; elapsed =
00:00:00.61 . Memory (MB): peak = 2141.250 ; gain = 0.004 ; free physical =
43808 ; free virtual = 150070
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit)
build 2258646
open_checkpoint: Time (s): cpu = 00:00:27 ; elapsed = 00:02:46 . Memory (MB):
peak = 2141.250 ; gain = 798.125 ; free physical = 43807 ; free virtual =
150069
Command: write_bitstream -force cpu.bit
Attempting to get a license for feature 'Implementation' and/or device
'xc7a100t'
INFO: [Common 17-349] Got license for feature 'Implementation' and/or device
'xc7a100t'
Running DRC as a precondition to command write_bitstream
INFO: [IP_Flow 19-234] Refreshing IP repositories
INFO: [IP_Flow 19-1704] No user IP repositories specified
INFO: [IP_Flow 19-2313] Loaded Vivado IP repository
'/CMC/tools/xilinx/Vivado_2018.2/Vivado/2018.2/data/ip'.
INFO: [DRC 23-27] Running DRC with 8 threads
WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG_VOLTAGE Design Properties:
Neither the CFGBVS nor CONFIG_VOLTAGE voltage property is set in the
current_design.  Configuration bank voltage select (CFGBVS) must be set to
VCCO or GND, and CONFIG_VOLTAGE must be set to the correct configuration
voltage, in order to determine the I/O voltage support for the pins in bank
0.  It is suggested to specify these either using the 'Edit Device
Properties' function in the GUI or directly in the XDC file using the
following syntax:

 set_property CFGBVS value1 [current_design]
 #where value1 is either VCCO or GND

 set_property CONFIG_VOLTAGE value2 [current_design]
 #where value2 is the voltage provided to configuration bank 0
```

```
Refer to the device configuration user guide for more information.
WARNING: [DRC PDRC-153] Gated clock check: Net U2/bitreg_reg[12][31] is a
gated clock net sourced by a combinational pin U2/reg_write_reg_i_2/O, cell
U2/reg_write_reg_i_2. This is not good design practice and will likely impact
performance. For SLICE registers, for example, use the CE pin to control the
loading of data.
WARNING: [DRC PDRC-153] Gated clock check: Net U7/E[0] is a gated clock net
sourced by a combinational pin U7/next_pc_reg[4]_i_2/O, cell
U7/next_pc_reg[4]_i_2. This is not good design practice and will likely
impact performance. For SLICE registers, for example, use the CE pin to
control the loading of data.
INFO: [Vivado 12-3199] DRC finished with 0 Errors, 3 Warnings
INFO: [Vivado 12-3200] Please refer to the DRC report (report_drc) for more
information.
INFO: [Designutils 20-2272] Running write_bitstream with 8 threads.
Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Writing bitstream ./cpu.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
21 Infos, 3 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_bitstream completed successfully
write_bitstream: Time (s): cpu = 00:00:14 ; elapsed = 00:00:39 . Memory (MB):
peak = 2621.090 ; gain = 479.840 ; free physical = 43739 ; free virtual =
150004
INFO: [Common 17-206] Exiting Vivado at Wed Dec  8 11:58:43 2021...
```

Synthesis Design

```
*** Running vivado
    with args -log cpu.vds -m64 -product Vivado -mode batch -messageDb
vivado.pb -notrace -source cpu.tcl


****** Vivado v2018.2 (64-bit)
  **** SW Build 2258646 on Thu Jun 14 20:02:38 MDT 2018
  **** IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018
    ** Copyright 1986-2018 Xilinx, Inc. All Rights Reserved.

source cpu.tcl -notrace
Command: synth_design -top cpu -part xc7a100tcsg324-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'
```

```
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device
'xc7a100t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 27286
---------------------------------------------------------------------------
----
Starting RTL Elaboration : Time (s): cpu = 00:00:02 ; elapsed = 00:00:05 .
Memory (MB): peak = 1468.594 ; gain = 86.727 ; free physical = 44440 ; free
virtual = 150698
---------------------------------------------------------------------------
----
INFO: [Synth 8-638] synthesizing module 'cpu'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:12]
INFO: [Synth 8-3491] module 'next_address' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/next_address.vhd:4' bound to instance 'U1' of component 'next_address'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:114]
INFO: [Synth 8-638] synthesizing module 'next_address'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/next_address.vhd:14]
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/next_address.vhd:36]
INFO: [Synth 8-256] done synthesizing module 'next_address' (1#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/next_address.vhd:14]
INFO: [Synth 8-3491] module 'pc_icache' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/pc_icache.vhd:7' bound to instance 'U2' of component 'pc_icache'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:115]
INFO: [Synth 8-638] synthesizing module 'pc_icache'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/pc_icache.vhd:19]
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/pc_icache.vhd:113]
INFO: [Synth 8-256] done synthesizing module 'pc_icache' (2#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/pc_icache.vhd:19]
INFO: [Synth 8-3491] module 'regfile' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/reg_file.vhd:8' bound to instance 'U3' of component 'regfile'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:116]
INFO: [Synth 8-638] synthesizing module 'regfile'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/reg_file.vhd:20]
```

```
INFO: [Synth 8-256] done synthesizing module 'regfile' (3#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/reg_file.vhd:20]
INFO: [Synth 8-3491] module 'signextension_mux' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/signextension.vhd:7' bound to instance 'U4' of component
'signextension_mux'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:117]
INFO: [Synth 8-638] synthesizing module 'signextension_mux'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/signextension.vhd:16]
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/signextension.vhd:22]
INFO: [Synth 8-256] done synthesizing module 'signextension_mux' (4#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/signextension.vhd:16]
INFO: [Synth 8-3491] module 'ALU' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:7' bound to instance 'U5' of component 'ALU'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:118]
INFO: [Synth 8-638] synthesizing module 'ALU'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:17]
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:23]
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:39]
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:75]
INFO: [Synth 8-256] done synthesizing module 'ALU' (5#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:17]
INFO: [Synth 8-3491] module 'datacache' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/datacache.vhd:6' bound to instance 'U6' of component 'datacache'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:119]
INFO: [Synth 8-638] synthesizing module 'datacache'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/datacache.vhd:14]
WARNING: [Synth 8-614] signal 'data_write' is read in the process but is not
in the sensitivity list
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/datacache.vhd:24]
```

```
INFO: [Synth 8-226] default block is never used
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/datacache.vhd:66]
INFO: [Synth 8-256] done synthesizing module 'datacache' (6#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/datacache.vhd:14]
INFO: [Synth 8-3491] module 'opcoderoute' declared at
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:7' bound to instance 'U7' of component 'opcoderoute'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:120]
INFO: [Synth 8-638] synthesizing module 'opcoderoute'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:14]
INFO: [Synth 8-256] done synthesizing module 'opcoderoute' (7#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:14]
INFO: [Synth 8-256] done synthesizing module 'cpu' (8#1)
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/cpu.vhd:12]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[25]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[24]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[23]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[22]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[21]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[20]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[19]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[18]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[17]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[16]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[15]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[14]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[13]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[12]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[11]
```

```
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[10]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[9]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[8]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[7]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[6]
---------------------------------------------------------------------------
----
Finished RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:07 .
Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical = 44442 ; free
virtual = 150700
---------------------------------------------------------------------------
----

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
---------------------------------------------------------------------------
----
Start Handling Custom Attributes
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished Handling Custom Attributes : Time (s): cpu = 00:00:03 ; elapsed =
00:00:07 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical =
44447 ; free virtual = 150705
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:03 ; elapsed =
00:00:07 . Memory (MB): peak = 1513.234 ; gain = 131.367 ; free physical =
44447 ; free virtual = 150705
---------------------------------------------------------------------------
----
INFO: [Device 21-403] Loading part xc7a100tcsg324-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
```

```
Parsing XDC File
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/constrs_1/import
s/lab5tedstuff/cpu.xdc]
Finished Parsing XDC File
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/constrs_1/import
s/lab5tedstuff/cpu.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while
reading constraint file
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/constrs_1/import
s/lab5tedstuff/cpu.xdc]. These constraints will be ignored for synthesis but
will be used in implementation. Impacted constraints are listed in the file
[.Xil/cpu_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in
[.Xil/cpu_propImpl.xdc] to another XDC file and exclude this new file from
synthesis with the used_in_synthesis property (File Properties dialog in GUI)
and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed =
00:00:00.01 . Memory (MB): peak = 1893.160 ; gain = 0.000 ; free physical =
44141 ; free virtual = 150398
------------------------------------------------------------------------------
----
Finished Constraint Validation : Time (s): cpu = 00:00:17 ; elapsed =
00:01:40 . Memory (MB): peak = 1893.160 ; gain = 511.293 ; free physical =
44226 ; free virtual = 150484
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Loading Part and Timing Information
------------------------------------------------------------------------------
----
Loading part: xc7a100tcsg324-1
------------------------------------------------------------------------------
----
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:17 ;
elapsed = 00:01:40 . Memory (MB): peak = 1893.160 ; gain = 511.293 ; free
physical = 44226 ; free virtual = 150484
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Applying 'set_property' XDC Constraints
------------------------------------------------------------------------------
----
```

```
---------------------------------------------------------------------------
----
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:17 ;
elapsed = 00:01:40 . Memory (MB): peak = 1893.160 ; gain = 511.293 ; free
physical = 44227 ; free virtual = 150485
---------------------------------------------------------------------------
----
INFO: [Synth 8-5546] ROM "bitreg_reg[31]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[30]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[29]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[28]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[27]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[26]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[25]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[24]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[23]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[22]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[21]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[20]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[19]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[18]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[17]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[16]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[15]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[14]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[13]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[12]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[11]" won't be mapped to RAM because it
is too sparse
```

```
INFO: [Synth 8-5546] ROM "bitreg_reg[10]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[9]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[8]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[7]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[6]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[5]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[4]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[3]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[2]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[1]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5546] ROM "bitreg_reg[0]" won't be mapped to RAM because it is
too sparse
INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared.
To prevent sharing consider applying a KEEP on the output of the operator
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/ALU.vhd:55]
INFO: [Synth 8-5546] ROM "d_cache_reg[31]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[30]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[29]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[28]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[27]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[26]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[25]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[24]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[23]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[22]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[21]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[20]" won't be mapped to RAM because it
is too sparse
```

```
INFO: [Synth 8-5546] ROM "d_cache_reg[19]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[18]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[17]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[16]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[15]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[14]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[13]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[12]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[11]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[10]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[9]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[8]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[7]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[6]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[5]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[4]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[3]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[2]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[1]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "d_cache_reg[0]" won't be mapped to RAM because it
is too sparse
INFO: [Synth 8-5546] ROM "reg_write" won't be mapped to RAM because it is too
sparse
WARNING: [Synth 8-327] inferring latch for variable 'next_pc_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/next_address.vhd:39]
WARNING: [Synth 8-327] inferring latch for variable 'reg_write_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:21]
```

```
WARNING: [Synth 8-327] inferring latch for variable 'reg_dst_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:22]
WARNING: [Synth 8-327] inferring latch for variable 'reg_in_src_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:23]
WARNING: [Synth 8-327] inferring latch for variable 'alu_src_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:24]
WARNING: [Synth 8-327] inferring latch for variable 'add_sub_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:25]
WARNING: [Synth 8-327] inferring latch for variable 'data_write_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:26]
WARNING: [Synth 8-327] inferring latch for variable 'logic_func_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:27]
WARNING: [Synth 8-327] inferring latch for variable 'alu_func_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:28]
WARNING: [Synth 8-327] inferring latch for variable 'branch_type_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:30]
WARNING: [Synth 8-327] inferring latch for variable 'pc_sel_reg'
[/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.srcs/sources_1/import
s/lab5/opcoderoute.vhd:31]
---------------------------------------------------------------------------
----
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:17 ; elapsed =
00:01:40 . Memory (MB): peak = 1893.160 ; gain = 511.293 ; free physical =
44218 ; free virtual = 150477
---------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
----
Start RTL Component Statistics
---------------------------------------------------------------------------
----
Detailed RTL Component Info :
+---Adders :
           2 Input     32 Bit       Adders := 2
           3 Input     32 Bit       Adders := 1
+---XORs :
```

```
           2 Input     32 Bit         XORs := 1
+---Registers :
                       32 Bit    Registers := 65
+---Muxes :
           2 Input     32 Bit        Muxes := 4
           4 Input     32 Bit        Muxes := 5
           2 Input      5 Bit        Muxes := 1
          14 Input      3 Bit        Muxes := 1
          14 Input      2 Bit        Muxes := 3
           9 Input      2 Bit        Muxes := 3
           5 Input      2 Bit        Muxes := 1
           4 Input      1 Bit        Muxes := 3
           2 Input      1 Bit        Muxes := 67
           9 Input      1 Bit        Muxes := 3
          14 Input      1 Bit        Muxes := 5
------------------------------------------------------------------------------
----
Finished RTL Component Statistics
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start RTL Hierarchical Component Statistics
------------------------------------------------------------------------------
----
Hierarchical RTL Component report
Module next_address
Detailed RTL Component Info :
+---Adders :
           2 Input     32 Bit       Adders := 2
+---Muxes :
           2 Input     32 Bit        Muxes := 1
           4 Input     32 Bit        Muxes := 2
           4 Input      1 Bit        Muxes := 2
Module pc_icache
Detailed RTL Component Info :
+---Registers :
                       32 Bit    Registers := 1
+---Muxes :
           2 Input      5 Bit        Muxes := 1
Module regfile
Detailed RTL Component Info :
+---Registers :
                       32 Bit    Registers := 32
+---Muxes :
           2 Input      1 Bit        Muxes := 32
Module signextension_mux
Detailed RTL Component Info :
+---Muxes :
           4 Input     32 Bit        Muxes := 1
```

```
           2 Input     32 Bit        Muxes := 1
Module ALU
Detailed RTL Component Info :
+---Adders :
           3 Input     32 Bit       Adders := 1
+---XORs :
           2 Input     32 Bit         XORs := 1
+---Muxes :
           4 Input     32 Bit        Muxes := 2
           2 Input     32 Bit        Muxes := 1
           2 Input      1 Bit        Muxes := 3
Module datacache
Detailed RTL Component Info :
+---Registers :
                       32 Bit    Registers := 32
+---Muxes :
           2 Input     32 Bit        Muxes := 1
           2 Input      1 Bit        Muxes := 32
Module opcoderoute
Detailed RTL Component Info :
+---Muxes :
          14 Input      3 Bit        Muxes := 1
          14 Input      2 Bit        Muxes := 3
           9 Input      2 Bit        Muxes := 3
           5 Input      2 Bit        Muxes := 1
           9 Input      1 Bit        Muxes := 3
          14 Input      1 Bit        Muxes := 5
           4 Input      1 Bit        Muxes := 1
------------------------------------------------------------------------------
----
Finished RTL Hierarchical Component Statistics
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Part Resource Summary
------------------------------------------------------------------------------
----
Part Resources:
DSPs: 240 (col length:80)
BRAMs: 270 (col length: RAMB18 80 RAMB36 40)
------------------------------------------------------------------------------
----
Finished Part Resource Summary
------------------------------------------------------------------------------
----
------------------------------------------------------------------------------
----
Start Cross Boundary and Area Optimization
```

```
---------------------------------------------------------------------------
----
Warning: Parallel synthesis criteria is not met
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[25]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[24]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[23]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[22]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[21]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[20]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[19]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[18]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[17]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[16]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[15]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[14]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[13]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[12]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[11]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[10]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[9]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[8]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[7]
WARNING: [Synth 8-3331] design opcoderoute has unconnected port
icacheout_combin[6]
INFO: [Synth 8-3333] propagating constant 0 across sequential element
(U7/\pc_sel_reg[1] )
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[31]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[30]) is unused and
will be removed from module next_address.
```

```
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[29]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[28]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[27]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[26]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[25]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[24]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[23]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[22]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[21]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[20]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[19]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[18]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[17]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[16]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[15]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[14]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[13]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[12]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[11]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[10]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[9]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[8]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[7]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[6]) is unused and
will be removed from module next_address.
WARNING: [Synth 8-3332] Sequential element (next_pc_reg[5]) is unused and
will be removed from module next_address.
```

WARNING: [Synth 8-3332] Sequential element (pc_reg[31]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[30]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[29]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[28]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[27]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[26]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[25]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[24]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[23]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[22]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[21]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[20]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[19]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[18]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[17]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[16]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[15]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[14]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[13]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[12]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[11]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[10]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[9]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[8]) is unused and will be removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[7]) is unused and will be removed from module pc_icache.

```
WARNING: [Synth 8-3332] Sequential element (pc_reg[6]) is unused and will be
removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (pc_reg[5]) is unused and will be
removed from module pc_icache.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][31]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][30]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][29]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][28]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][27]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][26]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][25]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][24]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][23]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][22]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][21]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][20]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][19]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][18]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][17]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][16]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][15]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][14]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][13]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][12]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][11]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][10]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][9]) is unused and
will be removed from module regfile.
```

```
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][8]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][7]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][6]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][5]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][4]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][3]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][2]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][1]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[31][0]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][31]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][30]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][29]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][28]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][27]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][26]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][25]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][24]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][23]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][22]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][21]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][20]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][19]) is unused and
will be removed from module regfile.
WARNING: [Synth 8-3332] Sequential element (bitreg_reg[30][18]) is unused and
will be removed from module regfile.
INFO: [Common 17-14] Message 'Synth 8-3332' appears 100 times and further
instances of the messages will be disabled. Use the Tcl command
set_msg_config to change the current settings.
```

```
---------------------------------------------------------------------------
----
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:40 ;
elapsed = 00:02:04 . Memory (MB): peak = 1908.418 ; gain = 526.551 ; free
physical = 44188 ; free virtual = 150450
---------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
----
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:47 ; elapsed
= 00:02:25 . Memory (MB): peak = 1908.426 ; gain = 526.559 ; free physical =
44066 ; free virtual = 150327
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Start Timing Optimization
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished Timing Optimization : Time (s): cpu = 00:00:49 ; elapsed = 00:02:27
. Memory (MB): peak = 1908.426 ; gain = 526.559 ; free physical = 44050 ;
free virtual = 150312
---------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
----
Start Technology Mapping
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
```

```
Finished Technology Mapping : Time (s): cpu = 00:00:51 ; elapsed = 00:02:28 .
Memory (MB): peak = 1926.363 ; gain = 544.496 ; free physical = 44057 ; free
virtual = 150318
-------------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
-------------------------------------------------------------------------------
----
Start IO Insertion
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Start Flattening Before IO Insertion
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Finished Flattening Before IO Insertion
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Start Final Netlist Cleanup
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Finished Final Netlist Cleanup
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Finished IO Insertion : Time (s): cpu = 00:00:51 ; elapsed = 00:02:29 .
Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical = 44057 ; free
virtual = 150319
-------------------------------------------------------------------------------
----

Report Check Netlist:
+------+------------------+-------+---------+-------+------------------+
|      |Item              |Errors |Warnings |Status |Description       |
+------+------------------+-------+---------+-------+------------------+
|1     |multi_driven_nets |      0|        0|Passed |Multi driven nets |
+------+------------------+-------+---------+-------+------------------+
```

```
---------------------------------------------------------------------------
----
Start Renaming Generated Instances
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished Renaming Generated Instances : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical =
44057 ; free virtual = 150319
---------------------------------------------------------------------------
----

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
----
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical =
44057 ; free virtual = 150319
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Start Renaming Generated Ports
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Finished Renaming Generated Ports : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical =
44057 ; free virtual = 150319
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
Start Handling Custom Attributes
---------------------------------------------------------------------------
----
---------------------------------------------------------------------------
----
```

```
Finished Handling Custom Attributes : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical =
44058 ; free virtual = 150319
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Start Renaming Generated Nets
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Finished Renaming Generated Nets : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical =
44058 ; free virtual = 150319
-------------------------------------------------------------------------------
----
-------------------------------------------------------------------------------
----
Start Writing Synthesis Report
-------------------------------------------------------------------------------
----

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    17|
|3     |LUT2   |     1|
|4     |LUT3   |    40|
|5     |LUT4   |     8|
|6     |LUT5   |    92|
|7     |LUT6   |   644|
|8     |MUXF7  |   193|
|9     |MUXF8  |    94|
|10    |FDCE   |  1541|
|11    |LD     |    18|
|12    |IBUF   |     2|
|13    |OBUF   |    14|
+------+-------+------+

Report Instance Areas:
+------+---------+------------------+------+
```

```
|      |Instance |Module            |Cells |
+------+---------+------------------+------+
|1     |top      |                  |  2665|
|2     |  U1     |next_address      |     5|
|3     |  U6     |datacache         |  1472|
|4     |  U2     |pc_icache         |   134|
|5     |  U3     |regfile           |   803|
|6     |  U4     |signextension_mux |    34|
|7     |  U7     |opcoderoute       |   193|
+------+---------+------------------+------+
-------------------------------------------------------------------------------
----
Finished Writing Synthesis Report : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.367 ; gain = 544.500 ; free physical =
44058 ; free virtual = 150319
-------------------------------------------------------------------------------
----
Synthesis finished with 0 errors, 0 critical warnings and 598 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:40 ; elapsed =
00:01:01 . Memory (MB): peak = 1926.367 ; gain = 164.574 ; free physical =
44114 ; free virtual = 150375
Synthesis Optimization Complete : Time (s): cpu = 00:00:51 ; elapsed =
00:02:29 . Memory (MB): peak = 1926.371 ; gain = 544.500 ; free physical =
44124 ; free virtual = 150386
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 324 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
  A total of 18 instances were transformed.
  LD => LDCE: 18 instances

INFO: [Common 17-83] Releasing license: Synthesis
110 Infos, 152 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:53 ; elapsed = 00:02:31 . Memory (MB):
peak = 1958.383 ; gain = 589.242 ; free physical = 44108 ; free virtual =
150370
WARNING: [Constraints 18-5210] No constraint will be written out.
INFO: [Common 17-1381] The checkpoint
'/nfs/home/o/o_dabaye/COEN316/code/lab5/lab5cpu/lab5cpu.runs/synth_1/cpu.dcp'
has been generated.
INFO: [runtcl-4] Executing : report_utilization -file
cpu_utilization_synth.rpt -pb cpu_utilization_synth.pb
report_utilization: Time (s): cpu = 00:00:00.07 ; elapsed = 00:00:00.19 .
Memory (MB): peak = 1982.402 ; gain = 0.000 ; free physical = 44107 ; free
virtual = 150370
INFO: [Common 17-206] Exiting Vivado at Wed Dec  8 11:49:11 2021...
```

OPCODEROUTE DOFILE

```
force icacheout_combin 00111100000000000000000000000000
run 2
force icacheout_combin 00000000000000000000000000100000
run 2
force icacheout_combin 00000000000000000000000000100010
run 2
force icacheout_combin 00000000000000000000000000101010
run 2
force icacheout_combin 00100000000000000000000000000000
run 2
force icacheout_combin 00101000000000000000000000000000
run 2
force icacheout_combin 00000000000000000000000000100100
run 2
force icacheout_combin 00000000000000000000000000100101
run 2
force icacheout_combin 00000000000000000000000000100110
run 2
force icacheout_combin 00000000000000000000000000100111
run 2
force icacheout_combin 00110000000000000000000000000000
run 2
force icacheout_combin 00110100000000000000000000000000
run 2
force icacheout_combin 00111000000000000000000000000000
run 2
force icacheout_combin 10001100000000000000000000000000
run 2
force icacheout_combin 10101100000000000000000000000000
run 2
force icacheout_combin 00001000000000000000000000000000
run 2
force icacheout_combin 00000000000000000000000000001000
run 2
force icacheout_combin 00000100000000000000000000000000
run 2
force icacheout_combin 00010000000000000000000000000000
run 2
force icacheout_combin 00010100000000000000000000000000
run 2
```